REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-5, 7-13, 15-18 and 20 are in the case. Claims 6, 14 and 19 have been canceled. Claims 1, 8, 15 and 20 have been amended.

Regarding the rejection of Claims 1, 6, 8, 14, 15, 19 and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura, independent Claims 1, 8 and 15 have been amended to overcome the rejection, with Claims 6, 8, 14 and 19 having been canceled thereby rendering the rejection moot with respect thereto. Claims 1 and 8 now recite a program counter copy register for storing a program memory address pointed to by a program counter as a return address from a debug monitor routine, while Claim 15 now recites the step of storing a memory address in a program counter copy register, wherein the address is reloaded into a program counter after execution of a debug routine.

These elements, which are neither shown nor suggested in the patent to Maemura, provide an important way for returning to the normal user program after executing a debug routine. Under normal conditions, a program counter copy register as recited may be operated to be continuously updated, for example with a current instruction fetch address. When a breakpoint occurs, the program counter copy register may then be locked, thereby storing the match instruction address. A long jump instruction may then be inserted to run the debug routine. At the end of the execution of the debug routine is finished, a return instruction may be executed, and the address stored in the program counter copy register used as the resume address. In this way, resumption of the normal program is assured. An additional benefit is that the program memory may be accessed during execution of the debug routing. This allows, for example, microprocessor execution condition information stored in the program memory to be outputted during debug.

By contrast, the patent to Maemura fails to even mention how to return to the breakpoint address and continue normal user program execution. Maemura is even unclear as to whether or how the breakpoint address might be saved. Thus, return to the user program may not occur. Even worse, according to Maemura's teachings when the background monitor executes a RETI (return from interrupt) to resume the breakpoint address (address "a"), Maemura's comparator 106 may find the address match again, and thereby trigger another breakpoint function. This would become an infinite loop. Still worse, Maemura's arrangement may not be able to return to the user program after entering the background monitor 105. Maemura's memory space switching circuit 107 appears only able to switch from user memory 102 to the background monitor 105 by the signal TRPAK 112 (break acknowledge terminal). After the breakpoint occurs, the program execution will jump to the background monitor 105, and appears to be unable to return to the user memory 102.

Thus, the elements added to Claims 1, 8 and 15 provide an important function that is neither shown nor suggested by the patent to Maemura. The other art of record is even less relevant. It is therefore respectfully submitted that for the above reasons independent Claims 1, 8 and 15 are allowable over Maemura and, indeed, all of the art of record, either considered alone or in any combination. Claim 20 now depends from Claim 15, and so is allowable for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 2, 3, 5, 10, 11, 13, 16, 17 and 18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Yishay et al., independent Claims 1, 8 and 15 have been amended to overcome the rejection, with Claims 2, 3 and 5 depending, directly or indirectly from Claim 1, Claims 10, 11 and 13 depending, directly or indirectly from Claim 8 and Claims 16, 17 and 18 depending, directly or indirectly from Claim 15.

The reasons for the allowability of Claims 1, 8 and 15 over the patent to Maemura are set forth above. The patent to Yishay et al. fails to cure the deficiencies of the patent to Maemura, apparently relating to comparison logic for breaking an address signal 54 into upper address signals and lower address signals. It fails to teach or suggest how to enter a breakpoint routine or how to return from it. In addition, it fails to teach or suggest the additional limitations found in these dependent claims. It is therefore respectfully submitted that all of the claims under this rejection are allowable over Maemura and Yishay et al. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 4, 9 and 12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Favor, independent Claims 1 and 8 have been amended to overcome the rejection, with Claim 4 depending from Claim 1 and Claims 9 and 12 depending from Claim 8. The reasons for the allowability of Claims 1 and 8 over the patent to Maemura are set forth above. The patent to Favor fails to cure the deficiencies of the patent to Maemura, apparently relating to an Intel x86 type instruction set translator, and having apparently nothing to do with single step breakpoint traps. In addition, it fails to teach or suggest the additional limitations found in these dependent claims. It is therefore respectfully submitted that all of the claims under this rejection are allowable over Maemura and Favor. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claim 7 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Jaggar, independent Claim 1 has been amended to overcome the rejection, with Claim 7 depending from Claim 1. The reasons for the allowability of Claim 1 over the patent to Maemura are set forth above. The patent to Jaggar fails to cure the deficiencies of the patent to Maemura, apparently relating to debug logic using a JTAG scan chain, and failing to teach or suggest a program counter

copy register for storing a program memory address pointed to by a program counter as a return address from a debug monitor routine. In addition, it fails to teach or suggest the additional limitations found in this dependent claim. It is therefore respectfully submitted that all of the claims under this rejection are allowable over Maemura and Jaggar. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

J. Dennis Moore
Attorney for Applicant(s)
Reg. No. 28,885

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
Phone: (972) 917-5646
Fax: (972) 917-4418